power at a level to [exchange] read and write memory information [with] in said memory integrated circuit during periods of data access activity, said power supplied during periods of no data access activity being less than said power supplied during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

14. (Amended) The dynamic power management device of Claim 4, wherein said power control means comprises a pulse width modulator circuit, [responsive to] said logic control means [for generating] causing said pulse width modulator circuit to generate a pulse width modulated signal having pulses with pulse widths proportional to said specified voltage output.

16. (Amended) The dynamic power management device of Claim 15, wherein said power control means further comprises a FET driver circuit coupled to said pulse width modulator circuit, said FET driver circuit generating a variable voltage having a voltage level proportional to the pulse widths of pulses in [response to] said filtered pulse width modulated signal.

Please cancel Claims 21-22.

23. (Amended) A dynamic power management device for supplying power to a solid state memory integrated circuit in a computer system having a power source [providing] supplying a substantially constant voltage, said dynamic power management device comprising:

power control means coupled to said power source for supplying a variable voltage to said memory integrated circuit, said variable voltage being less than or equal to

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said substantially constant voltage [provided] supplied by said power source; and

logic control means for generating address and control signals for said memory integrated circuit and for controlling said power control means to supply power to said memory integrated circuit at a level to maintain memory information in said memory integrated circuit during periods of no data access activity and to supply power at a level to [exchange] read and write memory information [with] in said memory integrated circuit during periods of data access activity, said power supplied during periods of no data access activity being less than said power supplied during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

SUMMARY OF EXAMINER INTERVIEW

An examiner interview was held by telephone on December 1, 1994. The main issue discussed was the 35 U.S.C. §112, first paragraph rejection of Claim 1. After discussion of Applicant's proposal to change the word "portions" to --elements-- in Claim 1, the Examiner stated that now that the meaning of Claim 1 was clear to him, he felt there was a 35 U.S.C. §112, first paragraph rejection because the phrase "supplying a variable voltage to said memory integrated circuit **independently** ..." (emphasis added) was not adequately described in the disclosure. He then stated that Applicant would have to file an amendment before he could consider any further discussion of this issue.

REMARKS

Reconsideration and allowance of Claims 1-20 and 23 is respectfully requested.

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